ABSTRACT OF THE DISCLOSURE

Parallel concatenated trellis-coding modulation is accomplished by producing coded bits (21) from uncoded bits and also producing an interleaved version (22) of the coded bits from the uncoded bits. A first coded bits-to-signal mapping (mapping 1) is applied to the coded bits to produce a first output signal (S_{11}), and a second coded bits-to-signal mapping (mapping 2) is applied to the interleaved version of the coded bits to produce a second output signal (S_{22}), wherein the second coded bits-to-signal mapping differs from the first coded bits-to-signal mapping.